ABSTRACT OF THE DISCLOSURE

To provide a driver circuit that is simple and possessing a small surface area. The driver circuit comprises a shift register circuit and a plurality of latch circuits. The shift register circuit is composed of a plurality of register circuits having a clocked inverter circuit and an inverter circuit connected in series. The plurality of digital data latch circuits has a first N-channel Tr and a second N-channel Tr of which the sources or the drains are connected in series, a P-channel Tr, and a data holding circuit. The clocked inverter circuit and the inverter circuit generate a timing signal on the basis of a clock signal and a start pulse to thereby feed the timing signal to the register circuit neighboring a register circuit and to a gate electrode of the first N-channel Tr and the P-channel Tr feeds a first electric voltage to the data holding circuit in accordance with a Res signal inputted to the gate electrode. The second N-channel Tr then takes in digital data on the basis of the timing signal to thereby output the digital data to the source or the drain of the first N-channel Tr. The timing signal outputted from the register circuit neighboring a register circuit is fed to the gate electrode of the first N-channel Tr.